REMARKS

The Office Action dated February 7, 2007 has been received and considered. In this response, claim 13 has been amended and new claim 54 has been added. The amendment to claim 13 does not narrow the scope of the claims and support for the amendment to claim 13 and the addition of new claim 54 can be found in the specification and drawings as originally filed. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Anticipation Rejection of Claims 13-29, 31-35, 37-40, 43-50, 52, and 53

At page 2 of the Office Action, claims 13-29, 31-35, 37-40, 43-50, 52, and 53 are rejected under 35 U.S.C. § 102(e) as being anticipated by Eifrig (U.S. Patent No. 6,748,020). This rejection is respectfully traversed.

Independent claim 13 presently recites the features of "a first processor to receive digital video data and provide parsed video data; and a second processor coupled to the first processor to access the parsed video data, the second processor including a video transcoder." The Office Action asserts that element 10 ("parsing/demux 10") of FIG. 1 of Eifrig represents the claimed "first processor" feature and further that element 30 ("core transcoding 30") of FIG. 1 of Eifrig represents the claimed "second processor" feature. The Applicants respectfully disagree. It is respectfully submitted that the Office's interpretation of element 10 and element 30 of Eifrig as two separate processors is suggested solely by the present application. Nowhere does Eifrig disclose that element 10 and element 30 each are implemented as a separate processor. In fact, Eifrig expressly teaches that element 10 and element 30 are implemented at the same Very Long Instruction Word (VLIW) core. *See, e.g., Eifrig*, col. 4, lines 6-33 ("a) MPEG transport stream decoding (on VLIW core)(10) [. . .] c) Core transcoding (on VLIW core)(30) [. . .]")(emphasis added).

It further is submitted that one of ordinary skill in the art will recognize that the parsing/demux (element 10) and the corresponding core transcoder (element 30) conventionally are implemented together as a single processor. Accordingly, as Eifrig fails to disclose a first processor that parses video data and a second processor that includes a transcoder and that

accesses the parsed video data, Eifrig necessarily fails to disclose at least the claimed features of "a first processor to receive digital video data and to provide parsed video data" and "a second processor coupled to the first processor to access the parsed video data, the second processor including a video transcoder" as recited by claim 13. Eifrig therefore fails to disclose each and every feature recited by claim 13.

Independent claim 53 recites the features of:

receiving, at a first processor, a data stream including video data;
parsing, at the first processor, the data stream to identify video data associated with a first channel;
packetizing, at the first processor, the video data associated with the first channel to generate the one or more packets, each packet having a video data payload and information related to the video data payload, wherein the video data payloads of the one or more packets represent a first channel of compressed video data having a characteristics represented by a first value;
receiving, at a second processor, the one or more packets; and
transcoding, at the second processor, the video data payloads of the one or more packets to generate a representation of a second channel of compressed video data having the characteristic represented by a second value.

As with claim 13, the Office Action asserts that element 10 ("parsing/demux 10") of FIG. 1 of Eifrig represents the first processor at which the claimed receiving, parsing, and packetizing operations are performed, and further that element 30 ("core transcoding 30") of FIG. 1 of Eifrig represents the second processor at which the claimed receiving and transcoding operations are performed. *Office Action*, p. 4. The Applicants respectfully disagree. As discussed above with respect to claim 13, the Office's interpretation of element 10 and element 30 of FIG. 1 of Eifrig as two separate processors is suggested solely by the present application. Further, as also discussed above, Eifrig specifically teaches that elements 10 and element 30 are implemented together in the same processor, rather than in different processors as provided by claim 54. Accordingly, as Eifrig fails to disclose a first processor that parses and packetizes video data and a second processor that includes a transcoder and that accesses the parsed and packetized video

data, Eifrig necessarily fails to disclose at least the claimed features of "parsing, at the first processor, the data stream to identify video data associated with a first channel;" "packetizing, at the first processor, the video data associated with the first channel to generate the one or more packets," and "transcoding, at the second processor, the video data payloads of the one or more packets to generate a representation of a second channel of compressed video data having the characteristic represented by a second value" as recited by claim 53. Eifrig therefore fails to disclose each and every feature recited by claim 53.

Independent claim 44 recites the features of:

a first data processor to:
receive one or more packets having a video data payload and information related to the video data payload, wherein the video data payloads of the one or more packets represent a first channel of compressed video data having a characteristic represented by a first value; and
transcode the video data payloads of the one or more packets to generate a representation of a second channel of compressed video data having the characteristic represented by a second value; and
a second data processor operably coupled to the first data processor, the second data processor to:
receive a data stream including video data at a first data processor;
parse the data stream to identify video data associated with a first channel;
packetize the video data associated with the first channel to generate the one or more packets; and
provide the one or more packets for reception by the first processor.

As discussed above with respect to claim 53, Eifrig fails to disclose or suggest one data processor to parse and packetize video data and a separate processor to transcode the parsed and packetized video data. Eifrig therefore fails to disclose or suggest the claimed first data processor feature and the claimed second data processor feature recited by claim 44. Eifrig therefore fails to disclose or suggest each and every feature of claim 44.

Eifrig further fails to disclose or even suggest the particular combinations of features recited by claims 14-40, 43, 45-50, 51, and 52 at least by virtue of their dependency from one of claims 13, 44, or 53. Moreover, these dependent claims recite additional novel features. For example, claim 14 recites the additional feature that the first processor is a general purpose processor. With respect to this feature, the Office merely points to element 10 of FIG. 1 of Eifrig. *Office Action*, p. 3. Contrary to the assertions of the Office Action, Eifrig fails to disclose or suggest element 10 is a general purpose processor.

In view of the foregoing, reconsideration and withdrawal of the anticipation rejection of claims 13-29, 31-35, 37-40, 43-50, 52 and 53 is respectfully requested.

Obviousness Rejection of Claim 36

At page 7 of the Office Action, claim 36 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Eifrig. This rejection is respectfully traversed.

Claim 36 presently depends from claim 53. As discussed above, Eifrig fails to disclose or suggest each and every feature of claim 53, so Eifrig necessarily fails to disclose or suggest the additional features of claim 36 at least by virtue of this dependency. Moreover, claim 36 recites additional novel features. Reconsideration and withdrawal of this rejection therefore is respectfully requested.

Addition of New Claim 54

New claim 54 has been added. New claim 54 depends from independent claim 13 and recites the features of "wherein the first processor and the second processor are integrated at a same package substrate." As discussed above, Eifrig fails to disclose or suggest the first and second processors of claim 13, and Eifrig further fails to disclose or suggest that the claimed first and second processors are integrated at the same package substrate as provided by claim 13.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present

application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Applicants believe no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-1835.

Respectfully submitted,

/Ryan S. Davidson/ May 7, 2007
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